

**In the claims:**

Rewrite the following claims as shown.

What is claimed is:

- sb B 7
- A2
1. (Amended) A method for designing an integrated circuit comprising:
- partitioning a design into a plurality of function blocks;
  - designing a first one of said plurality of function blocks employing Verilog to produce a first block design;
  - designing a second one of said plurality of function blocks employing SPICE to produce a second block design;
  - converting said first block design from Verilog to SPICE to produce a converted first block design comprising a file including a subcircuit name identified by ".SUBCKT" heading, at least one node name, at least one discrete circuit element description, at least one output signal name, and a ".ENDS" statement;
  - simulating operation of said converted first block design and said second block design; and
  - translating said converted first block design from SPICE to Verilog to produce a translated first block design.

- sb 17
- A3
3. (Amended) The method of claim 1 wherein said step of translating further comprises:
- changing said ".SUBCKT" heading in said converted first block design to "module".
4. (Amended) The method of claim 1 wherein said step of translating further comprises:
- changing said ".ENDS" statement in said converted first block design netlist to "endmodule".

- B1  
contd
5. (Amended) The method of claim 1 wherein said step of translating further comprises:  
deleting said at least one discrete circuit element description in said converted first block design.
6. (Amended) The method of claim 1 wherein said step of translating further comprises:  
defining a wire name corresponding to said at least one node name in said converted first block design.
7. (Amended) The method of claim 1 wherein said step of translating further comprises:  
identifying said at least one output signal name in said converted first block design and defining a Verilog output signal using said output signal name.
- A3
8. (Amended) The method of claim 1 wherein said step of translating further comprises:  
identifying said subcircuit name.
9. (Amended) The method of claim 8 wherein said step of translating further comprises:  
employing said subcircuit name as a module name.
10. (Amended) A method for translating a SPICE netlist to Verilog comprising:  
opening a SPICE file comprising a subcircuit name identified by a  
".SUBCKT" heading, at least one input signal name, at least one circuit element,  
at least one discrete circuit element description, an output signal name, and a  
.ENDS statement;  
translating said ".SUBCKT" heading in said SPICE file to "module";  
translating said ".ENDS" statement in said SPICE file to "endmodule";

*A3* *B1* *contd*  
translating said at least one circuit element in said SPICE file to Verilog  
format; and  
removing said at least one discrete circuit element description.

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*B1* *contd*  
12. (Amended) The method of claim 10 wherein said step of translating further  
comprises:

identifying said input signal name in said SPICE file and defining a  
Verilog wire employing said input signal name.

13. (Amended) The method of claim 12 wherein said step of identifying further  
comprises:

identifying said input signal name through a naming convention.

*PM*  
14. (Amended) The method of claim 12 wherein said step of identifying further  
comprises:

identifying said input signal name through a predefined delimiter.

15. (Amended) The method of claim 10 further comprising:

identifying said subcircuit name in said SPICE file.

16. (Amended) The method of claim 15 wherein said step of translating further  
comprises:

employing said subcircuit name as a Verilog module name.

17. (Amended) An integrated circuit produced by the steps of:

partitioning a design into a plurality of function blocks;

designing a first one of said plurality of function blocks employing  
Verilog to produce a first block design;

designing a second one of said plurality of function blocks employing  
SPICE to produce a second block design;

AM  
B1  
could  
converting said first block design from Verilog to SPICE to produce a converted first block design comprising a file including a subcircuit name identified by a ".SUBCKT" heading, at least one node name, at least one discrete circuit element description, at least one output signal name, and a ".ENDS" statement;

simulating operation of said converted first block design and said second block design; and

translating said converted first block design to Verilog to produce a translated first block design.

B1  
could  
19. (Amended) The integrated circuit of claim 17 wherein said step of translating further comprises:  
changing said ".SUBCKT" heading in said converted first block design to "module".

AS  
20. (Amended) The integrated circuit of claim 17 wherein said step of translating further comprises:  
changing said ".ENDS" statement in said converted first block design to "endmodule".

21. (Amended) The integrated circuit of claim 17 wherein said step of translating further comprises:  
deleting said discrete circuit element description in said converted first block design.

22. (Amended) The integrated circuit of claim 17 wherein said step of translating further comprises:  
defining a Verilog wire name corresponding to said at least one node name in said converted first block design.

- 23*  
*contd*
23. (Amended) The integrated circuit of claim 17 wherein said step of translating further comprises:  
identifying said at least one output signal name in said converted first block design and defining a Verilog output signal using said output signal name.
- 24*  
*contd*
24. (Amended) The integrated circuit of claim 17 wherein said step of translating further comprises:  
identifying said subcircuit name.
25. (Amended) The integrated circuit of claim 24 wherein said step of translating further comprises:  
employing said subcircuit name as a module name.
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#### Remarks

Reconsideration and further examination is respectfully requested. Claims 1-25 were originally presented for examination. Claims 1, 3-10, 12-17 and 19-25 have been amended. Claims 1-25 are presented for further examination.

The Examiner objected to figure 1 in the drawings. Applicant does not have knowledge that the process shown in figure 1 is prior art. No admissions have been made as such on the record. Hence, applicant has not amended figure 1.

Figure 5 was amended to include a period before "SUBCKT" and "ENDS". Support for this amendment is found in the syntax of the code listing of Appendix A of the application.

The Examiner objected to informalities in claims 3-5, 10, 19, 20 and 24 regarding reference to which block design the recited element exists in. These claims have been amended to recite the pertinent block. Claims 8 and 9 were objected to as ending in a semicolon rather than a period. These claims have been amended to correct the cited informalities.